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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

1. - 69. (cancelled)

70. (previously presented) A method for a first party to fabricate a semiconductor device, comprising:

receiving a sign-off prototype, the sign-off prototype generated by:

defining a physical design of a circuit while tracking an error in prediction of a timing value associated with one or more nets in the circuit;

determining a physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold; and

generating the sign-off prototype from the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold; and

after receiving the sign-off prototype, the first party performing:

generating a second physical design of the circuit from the sign-off prototype;

generating a GDS file from the second physical design;

having a mask set generated from the GDS file; and

having the semiconductor device fabricated using the mask set.

71. (original) The method of claim 70, wherein generating the second physical design of the circuit further comprises performing one or more of the following: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

72. (original) The method of claim 71, wherein the performing the placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design occurs substantially in parallel using a physical design tool.

73. (original) The method of claim 70, wherein the receiving the sign-off prototype further comprises receiving the sign-off prototype from a second party.

74. (previously presented) The method of claim 73, wherein generating the second physical design of the circuit from the sign-off prototype further comprises having the second party to perform additional interactive optimization on the sign-off prototype after receiving the sign-off prototype so the second party can collaborate in resolving problems identified in the sign-off prototype.

75. (original) The method of claim 70, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

(a) quadrisectioning the physical design into bins;

(b) localizing placement of cells and wires of the physical design into the bins;

(c) creating a profile of the wire lengths in each of the bins;

(d) calculating a plurality of errors in a prediction of timing values from the profile of the wire lengths for each bin respectively;

(e). comparing each of the plurality of errors in the prediction of the timing values with the predetermined threshold to determine if the timing value satisfies the predetermined threshold; and either:

further quadrisectioning the physical design and repeating (b through e); or

generating an interrupt if all of the plurality of errors in the prediction of the timing values for each of the bins satisfy the predetermined threshold.

76. (previously presented) A semiconductor device manufactured by a first party by:

receiving a sign-off prototype, the sign-off prototype generated by:

defining a physical design of a circuit while tracking an error in prediction of a timing value associated with one or more nets in the circuit;

determining a physical placement level of the circuit when the error in prediction

of the timing value satisfies a predetermined threshold; and

generating the sign-off prototype from the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold; and

after receiving the sign-off prototype, the first party performing:

generating a second physical design of the circuit from the sign-off prototype,

generating a GDS file from the second physical design;

having a mask set generated from the GDS file, and

having the semiconductor device fabricated using the mask set.

77. (original) The semiconductor device of claim 76, wherein generating the second physical design of the circuit further comprises performing one or more of the following: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design.

78. (original) The semiconductor device of claim 77, wherein the performing the placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design occurs substantially in parallel using a physical design tool.

79. (original) The semiconductor device of claim 76, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

(a) quadrisectioning the physical design into bins;

(b) localizing placement of cells and wires of the physical design into the bins;

(c) creating a profile of the wire lengths in each of the bins;

(d) calculating a plurality of errors in a prediction of timing values from the profile of the wire lengths for each bin respectively;

(e) comparing each of the plurality of errors in the prediction of the timing values with the predetermined threshold to determine if the timing value satisfies the predetermined threshold; and either:

further quadrisectioning the physical design and repeating (b through e); or

generating an interrupt if all of the plurality of errors in the prediction of the timing values for each of the bins satisfy the predetermined threshold.

80. (original) The semiconductor device of claim 76, wherein the receiving the sign-off prototype further comprises receiving the sign-off prototype from a second party.

81. (previously presented) The semiconductor device of claim 80, wherein generating the second physical design of the circuit from the sign-off prototype further comprises performing additional interactive optimization on the sign-off prototype after receiving the sign-off prototype so the second party can collaborate in resolving problems identified in the sign-off prototype.

82. – 100. (cancelled)

101. (previously presented) A method of performing a design of a circuit, comprising:

accessing a gate level design for said circuit;

creating a physical prototype from said gate level design, said creating of a physical prototype includes predicting of timing for said circuit and tracking an error in said predicting of timing; and

creating a physical design for said circuit, said creating of said physical design includes placing and routing elements of said circuit, said creating of a physical prototype is performed prior to said creating of said physical design.

102. (previously presented) A method according to claim 101, wherein:

said step of creating a physical design is performed using a physical design tool; and

said step of creating a physical prototype is performed without using said physical design tool.

103. (previously presented) A method according to claim 101, wherein said creating of said physical prototype comprises:

localizing placement of cells and wires;

creating a profile of wire lengths;

calculating an error in a prediction of a timing value from said profile of said wire lengths;

comparing said error in said prediction with a predetermined threshold; and

performing further placement if said error does not satisfy said predetermined threshold.

104. (previously presented) A method according to claim 101, wherein said creating of said physical prototype comprises:

defining a representation of said circuit based on said gate level design;

quadrisectioning said representation into bins;

localizing placement of cells and wires of said representation into said bins;

creating a profile of wire lengths in each of said bins;

calculating a plurality of errors in a prediction of timing values from said profile of said wire lengths for each bin respectively;

comparing each of said plurality of errors in said prediction of said timing values with a predetermined threshold; and

if said error does not satisfy said predetermined threshold, further quadrisectioning said representation and repeating said steps of localizing, creating, calculating and comparing.

105. (previously presented) A method according to claim 101, wherein said creating of said physical prototype further comprises analyzing congestion and power for said physical prototype.

106. (previously presented) A method according to claim 101, further comprising:

generating a GDS file from said physical design.

107. (previously presented) A method according to claim 101, further comprising:

generating a GDS file from said physical design;

having a mask set generated from the GDS file; and

having the semiconductor device fabricated using the mask set.

108. (previously presented) A method of performing a design of a circuit, comprising:

accessing a gate level design for said circuit;

creating a physical prototype from said gate level design, said creating of a physical prototype includes predicting of timing for said circuit; and

providing said physical prototype for a physical design process so that a physical design can be created for said circuit including placing and routing elements of said circuit, said creating of a physical prototype is performed prior to said step of providing.

109. (previously presented) A method according to claim 108, wherein:

said step of providing includes providing said physical prototype to a physical design tool; and

said step of creating a physical prototype is performed without using said physical design tool.

110. (previously presented) A method according to claim 108, wherein said creating of said physical prototype comprises:

localizing placement of cells and wires;

creating a profile of wire lengths;

calculating an error in a prediction of a timing value from said profile of said wire lengths;

comparing said error in said prediction with a predetermined threshold; and

performing further placement if said error does not satisfy said predetermined threshold.

111. (previously presented) A method according to claim 108, wherein said creating of said physical prototype comprises:

defining a representation of said circuit based on said gate level design;

quadrisectioning said representation into bins;

localizing placement of cells and wires of said representation into said bins;

creating a profile of wire lengths in each of said bins;

calculating a plurality of errors in a prediction of timing values from said profile of said wire lengths for each bin respectively;

comparing each of said plurality of errors in said prediction of said timing values with a predetermined threshold; and

if said error does not satisfy said predetermined threshold, further quadrisectioning said representation and repeating said steps of localizing, creating, calculating and comparing.

112. (previously presented) A method according to claim 108, wherein said creating of said physical prototype further comprises analyzing congestion and power for said physical prototype.

113. (previously presented) A computer-readable medium including computer code configured to perform the design of an integrated circuit, the computer code configures to perform a method comprising:

accessing a gate level design for said circuit;

creating a physical prototype from said gate level design, said creating of a physical prototype includes predicting of timing for said circuit; and

providing said physical prototype for a physical design process so that a physical design can be created for said circuit including placing and routing elements of said circuit, said creating of a physical prototype is performed prior to said step of providing.

114. (previously presented) A computer-readable medium according to claim 113, wherein:

said step of providing includes providing said physical prototype to a physical design tool; and

said step of creating a physical prototype is performed without using said physical design tool.

115. (previously presented) A computer-readable medium according to claim 113, wherein said creating of said physical prototype comprises:

localizing placement of cells and wires;

creating a profile of wire lengths;

calculating an error in a prediction of a timing value from said profile of said wire lengths;

comparing said error in said prediction with a predetermined threshold; and

performing further placement if said error does not satisfy said predetermined threshold.

116. (previously presented) A computer-readable medium according to claim 113, wherein said creating of said physical prototype comprises:

defining a representation of said circuit based on said gate level design;

quadrisectioning said representation into bins;

localizing placement of cells and wires of said representation into said bins;

creating a profile of wire lengths in each of said bins;

calculating a plurality of errors in a prediction of timing values from said profile of said wire lengths for each bin respectively;

comparing each of said plurality of errors in said prediction of said timing values with a predetermined threshold; and

if said error does not satisfy said predetermined threshold, further quadrisectioning said representation and repeating said steps of localizing, creating, calculating and comparing.

117. (previously presented) A computer-readable medium according to claim 113, wherein said creating of said physical prototype further comprises analyzing congestion and power for said physical prototype.

118. (previously presented) A computer system configured to perform the design of a circuit, the computer system comprising:

means for accessing a gate level design for said circuit;

means for creating a physical prototype from said gate level design, said creating of a physical prototype includes predicting of timing for said circuit; and

means for providing said physical prototype for a physical design process so that a physical design can be created for said circuit including placing and routing elements of said circuit, said creating of a physical prototype is performed prior to said step of providing.

119. (previously presented) A computer system according to claim 118, wherein:

said means for providing includes providing said physical prototype to a physical design tool; and

said means for creating does not use said physical design tool.

120. (previously presented) A computer system according to claim 118, wherein said means for creating of said physical prototype comprises:

means for localizing placement of cells and wires;

means for creating a profile of wire lengths;

means for calculating an error in a prediction of a timing value from said profile of said wire lengths;

means for comparing said error in said prediction with a predetermined threshold; and

means for performing further placement if said error does not satisfy said predetermined threshold.

121. (previously presented) A computer system according to claim 118 wherein said means for creating of said physical prototype comprises:

means for defining a representation of said circuit based on said gate level design;

means for quadrisectioning said representation into bins;

means for localizing placement of cells and wires of said representation into said bins;

means for creating a profile of wire lengths in each of said bins;

means for calculating a plurality of errors in a prediction of timing values from said profile of said wire lengths for each bin respectively;

means for comparing each of said plurality of errors in said prediction of said timing values with a predetermined threshold; and

means for, if said error does not satisfy said predetermined threshold, further quadrisectioning said representation and repeating said steps of localizing, creating, calculating and comparing.

122. (previously presented) A computer system according to claim 118, wherein said means for creating of said physical prototype further comprises means for analyzing congestion and power for said physical prototype.